

	Type	L #	Hits	S arch T xt	DBs	Time Stamp
1	BRS	L119	60885	TFT or "thin film transistor"	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:52
2	BRS	L120	195609 9	substrate or wafer	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:52
3	BRS	L121	1726	(polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:52
4	BRS	L125	727	upilex-s or upilex-vt or upilex-50ss or "UBE America"	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:52
5	IS&R	L127	994	(438/149).CCLS.	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:52

	Typ	L #	Hits	S arch T xt	DBs	Tim Stamp
6	IS&R	L129	304	(438/155).CCLS.	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:52
7	BRS	L131	315	(substrate base wafer bulk) with (polyphenylene near3 polyimide\$2)	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:52
8	BRS	L133	875	(substrate base wafer bulk) with (polyphenylene and polyimide\$2)	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53
9	BRS	L122	2	((substrate or wafer) near4 ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))) and (TFT or "thin film transistor")	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53
10	BRS	L123	28	(substrate or wafer) near4 ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53

	Typ	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L124	18	((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)) and (TFT or "thin film transistor")	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53
12	BRS	L126	9	(upilex-s or upilex-vt or upilex-50ss or "UBE America") and (TFT or "thin film transistor")	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53
13	BRS	L128	2	((438/149).CCLS.) and ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53
14	BRS	L130	1	((438/155).CCLS.) and ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53
15	BRS	L132	223	((substrate base wafer bulk) with (polyphenylene near3 polyimide\$2)) and (@ad<20000418 @rlad<20000418)	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53

	Type	L #	Hits	Search T xt	DBs	Tim Stamp
16	BRS	L134	597	((substrate base wafer bulk) with (polyphenylene and polyimide\$2)) and (@ad<20000418 @rlad<20000418)	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53
17	BRS	L135	152	((substrate base wafer bulk) with (polyphenylene and polyimide\$2)) and (@ad<20000418 @rlad<20000418)) and (chip semiconductor)	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/11 19:53

	Typ	L #	Hits	Search T xt	DBs	Tim Stamp
1	BRS	L1	60885	TFT or "thin film transistor"	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 10:44
2	BRS	L2	195609 9	substrate or wafer	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 10:45
3	BRS	L4	1726	(polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 10:45
4	BRS	L6	2	5 and 1	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 10:46
5	BRS	L5	28	2 near4 4	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 10:49

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L7	18	4 and 1	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 10:55
7	BRS	L8	727	upilex-s or upilex-vt or upilex-50ss or "UBE America"	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 10:55
8	BRS	L9	9	8 and 1	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 11:00
9	IS&R	L10	994	(438/149).CCLS.	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 11:00
10	BRS	L11	2	10 and 4	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 11:03

	Type	L #	Hits	S arch Text	DBs	Time Stamp
11	IS&R	L12	304	(438/155).CCLS.	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 11:03
12	BRS	L15	1	12 and 4	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2004/05/11 11:04

	Type	L #	Hits	Search T xt	DBs	Time Stamp
1	BRS	L1	60969	TFT or "thin film transistor"	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:57
2	BRS	L2	195737 3	substrate or wafer	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:57
3	BRS	L3	1730	(polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:57
4	BRS	L4	730	upilex-s or upilex-vt or upilex-50ss or "UBE America"	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:57
5	IS&R	L5	996	(438/149).CCLS.	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:57

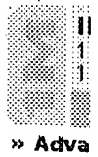
	Type	L #	Hits	Search T xt	DBs	Time Stamp
6	BRS	L6	316	(substrate base wafer bulk) with (polyphenylene near3 polyimide\$2)	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:57
7	BRS	L7	877	(substrate base wafer bulk) with (polyphenylene and polyimide\$2)	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:57
8	IS&R	L17	304	(438/155).CCLS.	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58
9	BRS	L8	2	((substrate or wafer) near4 ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))) and (TFT or "thin film transistor")	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58
10	BRS	L9	28	(substrate or wafer) near4 ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT ; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L10	18	((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide)) and (TFT or "thin film transistor")	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58
12	BRS	L11	9	(upilex-s or upilex-vt or upilex-50ss or "UBE America") and (TFT or "thin film transistor")	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58
13	BRS	L12	2	((438/149).CCLS.) and ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58
14	BRS	L13	223	((substrate base wafer bulk) with (polyphenylene near3 polyimide\$2)) and (@ad<20000418 @rlad<20000418)	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58
15	BRS	L14	1	((438/155).CCLS.) and ((polyphenylene near2 polyimide) or (poly-phenylene near2 polyimide))	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58

	Type	L #	Hits	S arch Text	DBs	Tim Stamp
16	BRS	L15	597	((substrate base wafer bulk) with (polyphenylene and polyimide\$2)) and (@ad<20000418 @rlad<20000418)	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58
17	BRS	L16	152	((substrate base wafer bulk) with (polyphenylene and polyimide\$2)) and (@ad<20000418 @rlad<20000418)) and (chip semiconductor)	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 12:58
18	IS&R	L18	651	(438/30).CCLS.	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 13:28
19	IS&R	L21	263	(438/152).CCLS.	USPAT; US-PG PUB; EPO; JPO; DERWE NT; IBM_T DB	2004/05/13 14:02

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Pages:5 - 12
[\[Abstract\]](#) [\[PDF Full-Text \(720 KB\)\]](#) **IEEE JNL**
2 Qualification testing of engineering thermoplastics for electrical distribution applications*Ferrito, S.J.;*Electrical Insulation and Dielectric Phenomena, 2002 Annual Report Conference on , 20-24 Oct. 2002
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Thin-film transistors on plastic and glass substrate: silicon deposited by microwave plasma ECR-CVD

[Lihong Teng](#) [Anderson, W.A.](#)

Dept. of Electr. Eng., State Univ. of New York, Buffalo, NY, USA

This paper appears in: **Electron Device Letters, IEEE**

Publication Date: June 2003

On page(s): 399 - 401

Volume: 24 , Issue: 6

ISSN: 0741-3106

Inspec Accession Number: 7701417

Abstract:

Thin-film transistors (TFTs) were fabricated on **polyimide** and glass substrate temperatures using microwave ECR-CVD deposited amorphous and nanocrystalline as active layers. The amorphous Si TFT fabricated at 200 /spl deg/C on the polyimide foil had a saturation region field effect mobility of 4.5 cm/sup 2//V-s, a linear region mobility of 5.1 cm/sup 2//V-s, a threshold voltage of 3.7 V, a subthreshold swing of 0.1 V/decade, and an ON/OFF current ratio of 7.9 /spl times/ 10/sup 6/. This large and high ON/OFF current ratio were attributed to the high-quality channel materials and less dangling bond defect states. Nanocrystalline Si TFTs fabricated on glass substrate at 400 /spl deg/C showed a saturation region mobility of 14.1 cm/sup 2//V-s, a linear region mobility of 15.3 cm/sup 2//V-s, a threshold voltage of 3.6 V, and an ON/OFF current ratio of 6.7 /spl times/ 10/sup 6/. TFT performance was mostly independent of substrate type when fabrication conditions were the same.

Index Terms:

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1 DC and microwave noise transient behavior of InP/InGaAs double heterojunction bipolar transistor (DHBT) with polyimide passivation
Yong Zhong Xiong; Geok-Ing Ng; Hong Wang; Fu, J.S.;

 Electron Devices, IEEE Transactions on , Volume: 48 , Issue: 10 , Oct. 2001
 Pages:2192 - 2197

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2 Current transient in polyimide-passivated InP/InGaAs heterojunction bipolar transistors: systematic experiments and physical model
Hong Wang; Geok-Ing Ng;

 Electron Devices, IEEE Transactions on , Volume: 47 , Issue: 12 , Dec. 2000
 Pages:2261 - 2269

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3 Polyimide Passivated AlGaIn-GaN HFETs With 7.65 W/mm at 18 GHz
Hampson, M.D.; Shen, S.-C.; Schwindt, R.S.; Price, R.K.; Chowdhury, U.; Wu, M.M.; Zhu, T.G.; Yoo, D.; Dupuis, R.D.; Feng, M.;

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[\[Abstract\]](#) [\[PDF Full-Text \(120 KB\)\]](#) IEEE JNL

4 Electron irradiation effects in polyimide passivated InP/InGaAs single heterojunction bipolar transistors
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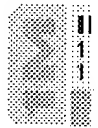
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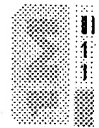
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